Design and Simulation of Phase Synchronizer for Adiabatic Quantum Flux Parametron Circuits

L. Camron Blackburn, Evan Golden, Alex Wynn, Andrew Wagner, and Neil Gershenfeld

***Abstract*—An adiabatic quantum flux parametron (AQFP) is a two-terminal superconducting device capable of amplifying or inverting digital input signals at near-kT energy dissipation. This ultra-low power device is desirable for myriad reasons, including high performance accelerator applications as CMOS processors become more and more limited by energy consumption. Promising performance results have been realized on AQFP processors; however, scaling these results to larger computing systems faces engineering challenges due to device density and power distribution. AQFP circuits require a multi-phase activation signal to propagate logic. If data is not properly aligned with the activation phase, it can be dropped or shifted to an incorrect phase and disrupt circuit operation. This work presents design and simulation of an activation phase synchronizer: a simple circuit that will accept data arriving on any phase and re-align it to a known phase of the subsequent cycle. The phase synchronizer can be useful for mitigating clock skew across clock domains or play an important role in asynchronous design where the arrival time of data may be unknown.**

***Index Terms*—Superconducting logic circuits, superconducting devices, superconducting integrated circuits, Josephson junctions, asynchronous logic.**

I. Introduction

THE Adiabatic Quantum Flux Parametron (AQFP) is a candidate for ultra-low energy computation, with near-$k_B T \ln 2$ energy dissipation per bit-operation [1]. The availability of relatively mature fabrication processes for superconducting integrated circuit fabrication [2], an extremely uniform cell design for AQFP circuits based on majority-inverter logic [3], and recent development of EDA tools for large-scale AQFP design [4], [5], [6] provide significant practical benefits for the realization of large-scale circuits and systems.

However, AQFP logic requires precise alignment of phase-overlapping AC activation signals as a basis for data propagation. This inherent synchrony presents a practical barrier to scaling to large systems due to the accumulation of phase-skew across designs of moderate size and complexity as the wavelength of the clock becomes comparable to the length of some interconnect paths. This problem is well known in the CMOS and superconductor electronics (SCE) communities, and has been a subject of active research since the advent of clocked systems [7], [8], [9], [10], [11]. On the scale of single-chip designs, a phase synchronizer is highly desirable to allow resilience against the significant timing uncertainty in cross-chip connections [5]. On the scale of larger systems, unless synchronization recovery of data across unknown phases can be achieved, scaling to large multi-chip modules envisioned by system architects [12], [13] may be intractable.

A phase synchronizer circuit, presented in this work, provides a solution to this problem by removing timing uncertainty on an incoming data signal. This is achieved by sampling the input signal across all possible arrival phases and propagating the data value to a known phase of a subsequent activation cycle. A weak constant QFP cell is introduced to behave as a filter on the input signal to prevent random noise from being amplified by the synchronizer.

II. Weak Constant QFP Cell

An AQFP, schematic shown in Fig. 1(a), consists of two superconducting loops, each with a single Josephson junction, that share a backbone and are inductively coupled to an AC activation signal. When the activation signal is on, a single flux quantum will be stored in one of the two loops, corresponding to a logical "1" or "0" state, directed by the polarity of the input current passing through each of the loops. A conventional AQFP buffer does not have a logically deterministic state for a null input condition; in the case of no current on the input line, it will amplify thermal noise and flux-bias offsets to generate pseudorandom data output [14]. This is an issue for a bit-level synchronizer which must sample the input across all phases and selectively propagate the meaningful data value. Therefore, to design a phase synchronizer, we first develop the notion of a weak-constant QFP cell.

In such a gate, a constant logic value will be given on the output if the signal on the input is null or weak, but in the presence of a data signal larger than a predetermined threshold, the constant output will be overwritten by the data bit. As shown in Fig. 1(b), the weak constant is created by introducing a slight asymmetry between the activation coupling coefficients, leading the QFP to preferentially favor one state. The coupling

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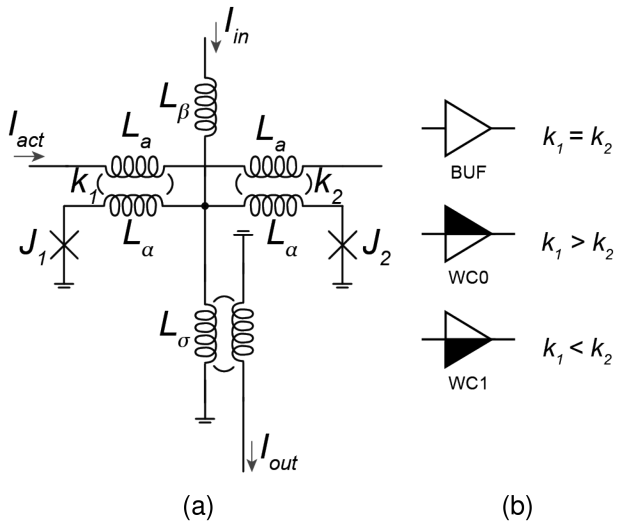

Fig. 1. (a) Generic AQFP schematic. (b) Circuit symbols for buffer (BUF), weak constant 0 (WC0), and weak constant 1 (WC1), and their associated modification to the schematic. A buffer has perfectly symmetric coupled loops, while the weak constant has unequal coupling constants.

coefficient is manipulated, as opposed to the size of the branch inductors, L_α, because this has a greater effect on the parametron state [15]. The strength of this offset can be controlled by the magnitude of the of asymmetry, while the default state of the weak constant QFP can be controlled by selecting which loop is larger.

This can be further understood by examining the current dynamics of the basic AQFP device. Writing Kirchoff's Current Law on each of the nodes of the QFP results in the following three equations

$$I_c \sin\phi_1 + \ell_\alpha(\phi_1 - \sigma - n_a k_1 \alpha) = 0 \tag{1}$$

$$\ell_\alpha(\phi_1 + \phi_2 - 2\sigma + n_a(k_2 - k_1)\alpha) + \ell_\beta(\beta - \sigma) - \ell_\sigma \sigma = 0 \tag{2}$$

$$I_c \sin\phi_2 + \ell_\alpha(\phi_2 - \sigma + n_a k_2 \alpha) = 0 \tag{3}$$

where I_c is the critical current of the junctions, $\ell = \frac{\Phi_o}{2\pi}\frac{1}{L}$ for each inductor, ϕ_1 and ϕ_2 are the phase differences across each junction, β, α, and σ are the phase differences across the input, loop, and output inductors, respectively; n_a^2 is the activation transformer ratio, which we've assumed to always be symmetric in both loops, and k_1 and k_2 are the coupling constants which can vary. We can reorganize these equations to be expressed in terms of $\phi_+ = \frac{1}{2}(\phi_1 + \phi_2)$ and $\phi_- = \frac{1}{2}(\phi_1 - \phi_2)$, and solve (2) for σ to reduce the three equations to two and get the following result.

$$2I_c \sin\phi_+ \cos\phi_- + \ell_+\left(\phi_+ + \frac{n_a(k_2 - k_1)}{2}\alpha - \frac{\ell_\beta}{\ell_\alpha(k_\sigma - 2)}\beta\right) = 0 \tag{4}$$

$$2I_c \cos\phi_+ \sin\phi_- + \ell_\alpha(2\phi_- - n_a(k_2 + k_1)\alpha) = 0 \tag{5}$$

where $\ell_+ = \frac{2\ell_\alpha(k_\sigma - 2)}{k_\sigma}$ and $k_\sigma = (2\ell_\alpha + \ell_\beta + \ell_\sigma)/\ell_\alpha$. These equations guide the operation of the parametron.

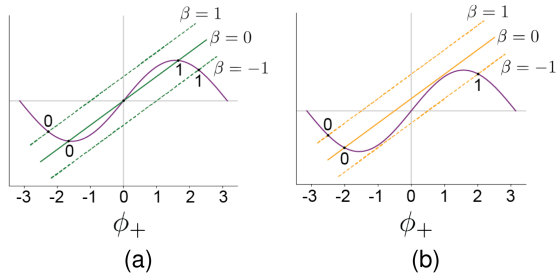

Fig. 2. Solutions to (4) for (a) the buffer when $k_1 = k_2$ and (b) the weak constant 0 when $k_1 > k_2$. The logical value that each solution corresponds to is labeled on the graphs. Dashed lines above and below correspond to input 1 ($\beta = 1$) and 0 ($\beta = -1$), respectively; and the solid line is state of the parametron when activated with no input ($\beta = 0$).

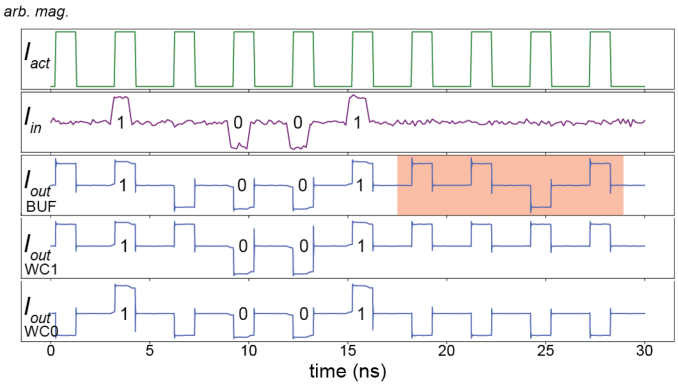

Fig. 3. Simulated output of a single buffer, weak constant 1 (WC1), and weak constant 0 (WC0). Gaussian random noise has been added to the input signal to highlight proper operation of each cell: the buffer amplifies the pseudorandom noise when no data value is passed, while WC0 and WC1 default to 0 or 1 respectively.

The QFP will be storing information when it's in the double potential state, *i.e.* when the activation phase difference $\alpha = \pm\frac{\pi}{n_a(k_2+k_1)}$ [16]. This corresponds to a solution for (5) when $\phi_- = \pm\pi$ and we can therefore reduce our analysis to (4) when $\phi_- = 0, \pm\pi$. As shown in Fig. 2 the solution of (4) can be visualized as the intersection of a sine function with a straight line. Provided the slope, ℓ_+, is less than one, there are up to three possible solutions: high or low ϕ_+ corresponding to a logical 1 or 0, and the solution around 0 which corresponds to an energy maxima.

The state that the parametron settles in depends on the linear shift provided by the α and β term in the line equation. If $k_1 = k_2$, as is the case for the buffer, then the state of the gate depends entirely on the input value. If no input value is given, it will randomly slip into either high or low state. However, if the coupling constants are not equal, then the parametron state also depends on the activation signal, and it is this asymmetry that produces the biased weak constant cell. In other words, the extra coupling between the activation transformer behaves as a current source in one of the parametron loops and causes the output to favor one side. Additionally, optimization of the constant cell from a potential energy perspective has been done by Ando [15].

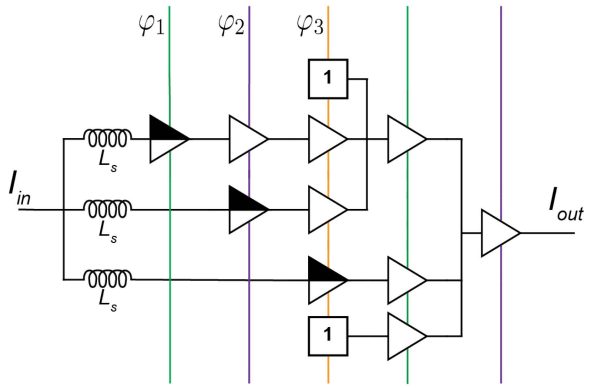

Fig. 4. Phase synchronizer circuit schematic. Majority operations are indicated by the connection of three nodes, thus a constant 1 joined with two inputs results in an OR operation. The activation signal for each cell is labeled with φ_1, φ_2, φ_3 and cycles through each stage from left to right, as the color indicates. Each QFP cell requires 2 JJs, the circuit has 24 JJs in total.

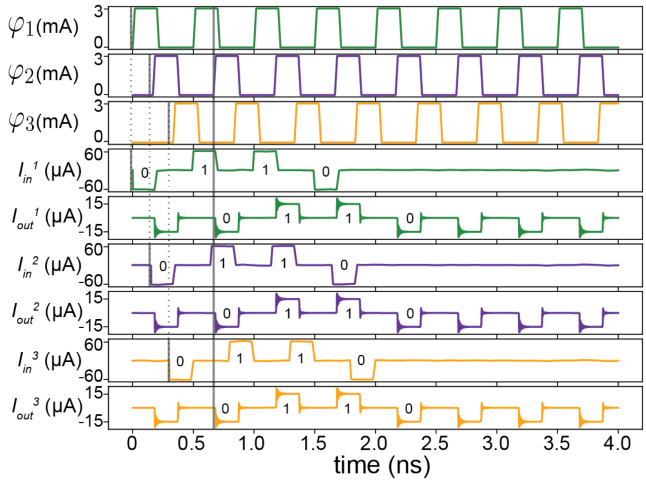

Fig. 5. SPICE level simulation of the phase synchronizer circuit at 1 GHz activation cycle. The input was shifted to align with the first, second, and third phase, I_{in1}, I_{in2}, I_{in3} respectively, while the output remains aligned at the second phase of the next activation cycle. A Gaussian noise source was included on the input signal. L_s was minimized to 18 pH for isolation of back propagation noise. The operational margin on the activation amplitude is $[-16\%, +8\%]$ centered around 3 mA.

Fig. 3 demonstrates simulation of both weak constant cells compared to a conventional AQFP buffer. The SPICE level simulation was performed with Cadence SPECTRE simulator with support for Josephson junction dynamics. A 1 μA Gaussian noise source was included in the input signal to highlight the distinction between the weak constant cells and the buffer: the buffer amplifies the noise source (highlighted in red), while the weak constant maintains its constant output. For an input magnitude of 15 μA, the operational range of WC0 was found to be $k_2/k_1 = [1.01, 1.36]$; a ratio larger than this will result in a full constant cell. The inverse is true for the WC1 cell.

III. Synchronizer Design

A. Requirements

Due to the two-terminal nature of the parametron device, AQFP logic requires a multi-phase activation signal with a minimum of 3 phases. In a circuit network, a single QFP device cycles through states of (i) **receiving** data while the activation signal is brought high, (ii) **propagating** data at the output/input while the activation signal remains high, and (iii) **blocking** data while the activation signal is low to prevent back propagation of data. Therefore, the arrival of data must align with a QFP in the receiving state.

If the data arrival phase is unknown, then a bit-level phase synchronizer must perform the following tasks: (i) accept data input during any time of the activation cycle (whether it aligns with a single phase or is spread between multiple); (ii) remove temporal uncertainty associated with the input bit by propagating the value to an output signal of a known phase; (iii) output a predetermined value in the absence of an input signal.

We designed a phase synchronizer with a multiplexer topology that samples each input phase through a weak constant zero cell and outputs the logical OR of all input phases, shown in Fig. 4. The circuit meets the phase synchronizer requirements for a three-phase clock, although the general design could be extended to a larger phase count if needed.

B. Simulation

Operation of the phase synchronizer was verified in simulation with Cadence SPECTRE tools, shown in Fig. 5. Notably, the current input signal to the phase synchronizer must be large enough to split across all of the feedback inductors and overcome the threshold of the weak constant values. In simulation with 18 pH inductors on each of the input branches, a 60 μA input amplitude was required; compared to the 15 μA logic-level currents typically used in AQFP circuits. Therefore, to drive the phase synchronizer with AQFP logic, a multi-turn transformer could be added to the input to passively amplify the current. Alternatively, if area is more of a concern than energy, a DC-bias amplifier, such as a SQUID amplifier [17] or nanocryotron [18], could be added to the input.

For VLSI design, the phase synchronizer is an important circuit to include at I/O ports of AQFP logic units and could demand a higher current level as a design requirement; similar to I/O versus logic voltage levels in CMOS IC design.

C. Circuit Measurement

We demonstrate initial fabrication and testing of the weak constant cell. The circuits were fabricated in the SFQ5ee process [2], and tested with a liquid Helium dunk probe at kHz frequencies, using an Octopux measurement system [19]. Fig. 7 shows a micrograph of our AQFP buffer (7(a)) along side a WC0 cell (7(b)). The asymmetry between the coupling constants was achieved by briefly routing the activation line (red highlighted line in Fig. 7) away from the right arm inductor of the QFP.

The output of the gates was measured by directly coupling a DC-bias SQUID to each of the output lines. The results from testing are shown in Fig. 6. Ideally, we would expect the buffer to output pseudorandom values when activated with 0 μA on the input line, as discussed in section II; however, in reality, the gray

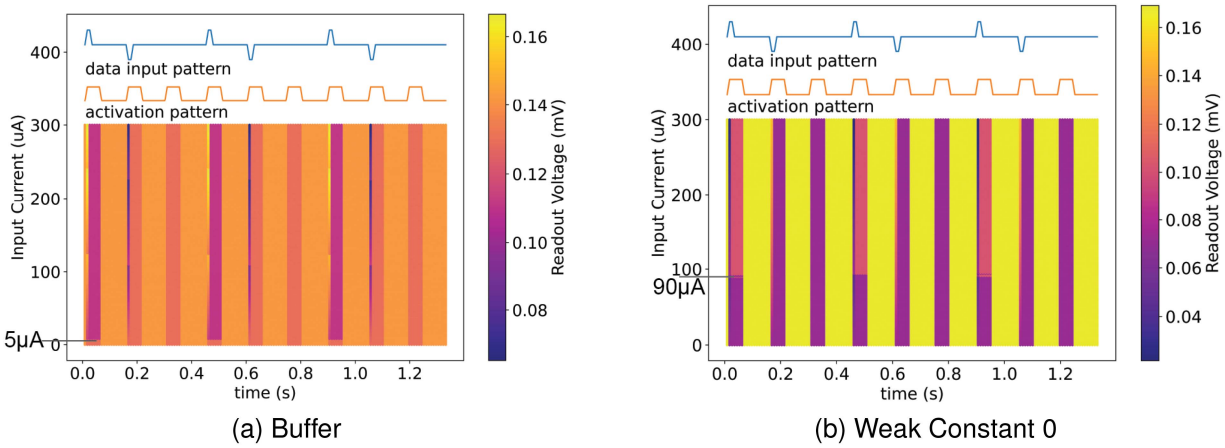

Fig. 6. Input margin measurements of the (a) AQFP buffer and (b) weak constant. The data and activation pattern are shown across the top. When the gate's data threshold is reached, the output voltage begins switching with the data pattern: 5 μA for the buffer, 90 μA for the weak constant 0 cell.

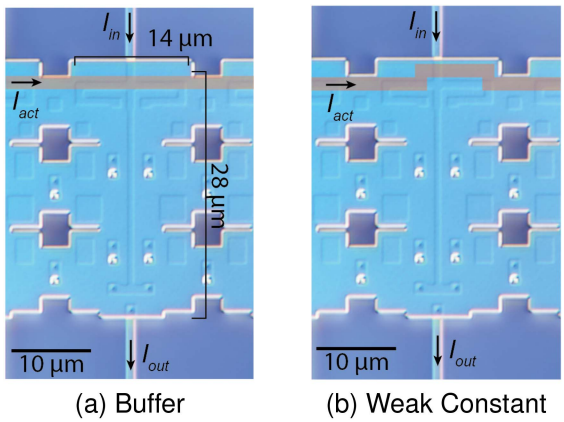

Fig. 7. A polarized optical micrograph of (a) the buffer and (b) the weak constant is shown next to each device's test data. The activation signal is coupled through an inductor segment which is not pictured on the micrograph metal layer, but drawn in red to highlight the coupling asymmetry which is critical to the weak constant operation.

zone of the buffer is not located perfectly at 0 μA, presumably due to flux trapping noise in the circuit and fabrication tolerances [20]. In this sense, all buffer cells can indirectly behave as weak constants, but a weak constant is distinct in it's purposeful asymmetric design and repeatable bias.

The data threshold for our fabricated buffer cell is around 5 μA, and 90 μA for the weak constant. Given that the current level used in AQFP logic is around 15–30 μA, the 90 μA threshold is much too high of an operating point for the weak constant. This is most likely arises from too large of an asymmetry between the activation couple constants. Further optimizations underway in current work.

IV. Applications

We foresee two important applications for the phase synchronizer circuit: clock skew mitigation and asynchronous or temporal logic design.

If it is known that data will arrive at some point during an activation cycle, the phase synchronizer can remove phase uncertainty by propagating the data value to a known phase of a future activation cycle. This can allow for wider clock margins at parts of the circuit which are highly sensitive to clock skew, such as long interconnects or unbalanced logic operations.

Additionally, the phase synchronizer can operate as a coincidence buffer by flagging the arrival of data across any amount of time because it will always output 0 until a data value 1 arrives. This is useful for (i) dual rail asynchronous logic or (ii) temporal race logic, where a bit is always represented with a high level value, and it's value is determined by (i) the wire it's on or (ii) the time is arrives, respectively. Slight adjustments can be made to the design (replacing WC0 with WC1 and inverting the ORs), to have the synchronizer flag the presence of low current level data. This provides a first step to converting the multi-phase ac-biasing from a clock signal that's integral to the AQFP logic operation into a power grid with the logic operating more flexibly at an abstraction layer above it.

V. Conclusion

We demonstrated the design and simulation of a phase synchronizer circuit and provided initial fabrication and testing results of the weak constant QFP cell, a key component of the synchronizer circuit. As we have motivated future applications, the phase synchronizer has the potential to be a critical component to scaling AQFP designs to larger area, more complex systems, or novel asynchronous implementations of the logic family. Future work aims to further optimize design of the weak constant cell and develop a layout and footprint of the full phase synchronizer circuit for fabrication and testing, while continuing to explore its integration with larger AQFP logic circuits.

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