The history of computers
• An automatic computing machine must have:
  • A store for the numbers (memory)
  • A device for performing arithmetic operations (ALU)
  • A device for causing the operations of the machine (CU)
  • An input and output device (Mouse, keyboard, screen)
First Generation: The Manchester Computer

- The world’s first stored-program electronic digital computer

- Executed its first program on June 21st in 1948.

- Designed and constructed by Macheester University

- Ferranti Ltd. was given rights to produce and sell a commercial version of the machine (Manchester mark I)
The Most Important Step: Integrated Circuits

- The introduction of integrated circuits led to the third generation of computers

- Mini-machines made out of logic gates

- Small scale integrated circuits
tiny13 AVR chip
The AVR fairy tale
how the west was won and how we got there
Atmel Norway AS - today

- 120 employees in Trondheim
- 50 employees abroad
- 35 products in production
- 12,000,000 chips/month
- 4.5 chips pr. second
- Own 100% by Atmel Corp
  - Nasdaq: ATML
Key AVR Features – the sales pitch

- Flash and EEPROM, both in-system programmable
- Highest performance, low power 8-bit MCU
- Excellent code density in C and assembly
- A broad family of MCUs - 1K to 256K Bytes flash
- High integration
8-Pin Family Details

- Tiny25/45/85
  - Three Pin and functionally compatible devices
  - 4-channel 10-bit ADC
    - Differential channels with 10/20X Gain
  - High frequency (200 KHz) 8-bit PWM
  - Pin-change interrupt on all I/O-pins
  - Low power consumption
    - 100 nA power down mode
  - debugWIRE On-chip Debug

- Tiny13
  - Pin compatible with Tiny25/45/85
  - 4-channel 10-bit A/D
  - Pin-change interrupt on all I/O pins
  - Low power consumption
  - 100 nA power down mode
  - debugWIRE On-chip Debug

<table>
<thead>
<tr>
<th>Device</th>
<th>Flash</th>
<th>RAM</th>
<th>EEPROM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tiny13</td>
<td>1K</td>
<td>64</td>
<td>64</td>
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<tr>
<td>Tiny25</td>
<td>2K</td>
<td>128</td>
<td>128</td>
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<tr>
<td>Tiny45</td>
<td>4K</td>
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<tr>
<td>Tiny85</td>
<td>8K</td>
<td>512</td>
<td>512</td>
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</table>
14-pin family highlights

- Pin/Functionally compatible devices
- 8-channel 10-bit ADC
  - 7 Differential channels with 1/8/20X Gain
- Pin-change interrupt on all I/O-pins
- Low power consumption
  - 100 nA power down mode
  - 1.8 to 5.5 volt operation
- Internal 8 MHz RC oscillator
- debugWIRE On-chip Debug

<table>
<thead>
<tr>
<th>Device</th>
<th>Flash</th>
<th>RAM</th>
<th>EEPROM</th>
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<tbody>
<tr>
<td>Tiny24</td>
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<tr>
<td>Tiny44</td>
<td>4K</td>
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<tr>
<td>Tiny84</td>
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<td>512</td>
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</tbody>
</table>
20-pin family

- **Tiny26/46/86**
  - 11-channel 10-bit A/D
    - Differential Channels with 10/20X gain
  - High frequency (200 KHz) PWM
  - Debugwire On-Chip Debug (Tiny45/85)
  - 8 MHz Internal RC
- **Tiny2313**
  - Hardware USART
  - Interrupt on pin-change on all I/O
  - USI gives hardware support for SPI/TWI
  - Low power consumption
    - 100 nA Power down mode
  - DebugWIRE On-Chip Debug

<table>
<thead>
<tr>
<th>Device</th>
<th>Flash</th>
<th>RAM</th>
<th>EE</th>
<th>VCC</th>
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<tr>
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<tr>
<td>Tiny46</td>
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<tr>
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<td>128</td>
<td>128</td>
<td>1.8 – 5.5V</td>
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The Development of an AVR Microcontroller
Developing a Microcontroller

1. Specification
   - Digital design and Verification
   - Analog design and Verification
   - Digital/analog Co-verification
   - Lay-out
   - Final Verification
Digital Design

- CPU, Interrupt Controller, DMA, Peripheral Functions etc.
- Developed in HDL (Verilog)
- Verification on HDL model
- Module Reuse and Improvement
- IP Modules
- HDL synthesis

- Verilog Example:

```verilog
always @ ( posedge clk )
begin  // Register write
  if((adr==UCSRB_adr)&iowe)
    begin
      rxcie <= `DD dbus[7];
      txcie <= `DD dbus[6];
      udrie <= `DD dbus[5];
      rxen  <= `DD dbus[4];
      txen  <= `DD dbus[3];
      chr9  <= `DD dbus[2];
    end
end
```
Analog Design

- Memories, ADCs, DACs, Regulators, Oscillators, PADs, etc.
- Analog modules implemented as schematic drawings
- Digital Interfaces
- IP Modules
- Process shrink (libraries) 0.35µ, 0.25µ, 0.18µ, 0.13µ
Lay Out

- The Digital Design has been synthesized to a low level representation

- The Digital Design has to be merged with the Analog Design

- The Lay Out must meet performance and size constraints
Silicon Die
Packaging

- **Die**
  - All devices available in Die Form
- **Micro Lead Frame Packaging**
  - Low cost package technology
  - Very good noise immunity substrate connected to ground
  - Smallest standard package available
  - Near chip-scale package size; Save up to 69% of board space

<table>
<thead>
<tr>
<th>TQFP size</th>
<th>MLF size</th>
<th>TQFP area</th>
<th>MLF area</th>
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<tbody>
<tr>
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<td>5 x 5</td>
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<tr>
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<td>9 x 9</td>
<td>256</td>
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<tr>
<td></td>
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<td>32 %</td>
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</tbody>
</table>
The future
Trends into the future

- **Shrink**
  - Size decrease will continue
  - Lower production cost and end user price

- **Lower power**
  - Today 1.8V operation
    - 1 Li cell or 2 AA/AAA batteries to run
  - 0.9V technology will be introduced
    - 1 AA/AAA battery to run

- **On-chip debug**
  - The end of expensive in-circuit emulators

- **Open source**
  - Linux OS
  - User interaction. [www.avrfreaks.net](http://www.avrfreaks.net)