



```

matCons[{{wiremod, wiremod, wiremod, wiremod, wiremod},
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{wiremod, split, fanOut, wiremod},
{{1, 4}, {2, 6}, {3, 3}, {4, 5}, {5, 1}, {6, 2}},
{split, serialMult[5], wiremod, sink},
{{1, 2}, {2, 1}, {3, 3}, {4, 4}},
{wiremod, adder, wiremod},
{{1, 3}, {2, 2}, {3, 1}},
{switchnonblocking}, {1, 1}, {wiremod}}]
  
```



image: Peter Schmidt-Nielsen © 2011

Visual dataflow programming of asynchronous logic automata.